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Patent No. 3214256

(54) [Title of the Invention]

ELECTRON PULSE EMISSION DEVICE AND DISPLAY DEVICE

(57) [Claims]

[Claim 1] An electron pulse emission device comprising a supporting substrate, a first electrode formed on said supporting substrate, a ferroelectric layer formed on top of said first electrode, a second electrode formed on top of said ferroelectric layer without being in contact with said first electrode, a third electrode facing toward said second electrode across a space, a means for applying a positive DC bias with regard to said first electrode to said third electrode, and a means for applying an AC pulse voltage between said first electrode and said second electrode to induce polarization inversion in said ferroelectric layer, wherein said electron pulse emission device is characterized by intermittently emitting electrons from the surface of said second electrode toward said third electrode.

[Claim 2] The electron pulse emission device according to claim 1, wherein said supporting substrate is a semiconductor substrate of one channel type and said first electrode consists of a diffusion layer of the other channel type, formed on said semiconductor substrate.

[Claim 3] A display device comprising a supporting substrate, a plurality of first electrodes formed on said supporting substrate, a ferroelectric layer formed on top of said first electrodes, a plurality of second electrodes formed on top of

said ferroelectric layer without being in contact with said first electrodes and in an orthogonal direction to said first electrodes, and an isolation layer formed on top of said second electrodes, said isolation layer having openings at the intersections of said plurality of first electrodes and said plurality of second electrodes, wherein said supporting substrate is placed opposite to a transparent substrate across a space, said transparent substrate facing toward said second electrodes across the space and having a transparent conductive layer and a phosphor layer formed thereunder, wherein said display device further comprises a means for applying a positive DC bias with regard to said first electrodes to said transparent conductive layer and a means for applying an AC pulse voltage between each said first electrode and each said second electrode to induce polarization inversion in said ferroelectric layer, wherein said display device is characterized by intermittently emitting electrons from the exposed surfaces of said second electrodes toward said transparent conductive layer.

[Claim 4] The display device according to claim 3, wherein said supporting substrate is a semiconductor substrate of one channel type and said first electrode consists of a diffusion layer of the other channel type, formed on said semiconductor substrate.

[Claim 5] The display device according to claim 4, wherein said supporting substrate is provided with a drive circuit for supplying electrical signals to said plurality of first electrodes and said plurality of second electrodes.

[Claim 6] The display device according to claim 3, 4, or 5, wherein said plurality of first electrodes and said plurality of second electrodes intersect such that the intersections in a column (or row) are a half pitch off the positions of the intersections in an adjacent column (or row).

[Claim 7] The display device according to claim 3, 4, 5, and 6 wherein partitions of two or more kinds of phosphor films corresponding to the intersections of said plurality of first electrodes and said plurality of second electrodes are formed in a matrix on said transparent substrate.

[Detailed Description of the Invention]

[0001]

[Field of Industrial Application] The present invention relates to an electron pulse emission device that uses the surface of one electrode of a capacitance device employing a ferroelectric layer or a dielectric layer with a high dielectric constant for capacitive isolation as the surface for cold cathode electron emission and a display device employing the electron pulse emission device.

[0002]

[Prior Art] The speed at which electrons move in a solid element is at most on the order of one thousandth of light velocity and solid elements have limitations in their operating speed. In view of their properties, the solid elements also have drawbacks that they are susceptible to radioactive rays and temperature change. Recently, to overcome such drawbacks of the solid elements, attempts to integrate micro vacuum tubes into a solid

element by way of a micro-fabrication technique have actively been made.

[0003] Various shapes of cold cathodes have been employed in the micro vacuum tubes and, among them, needle electrodes, which can achieve a high density of electron emission over 1000 A/Cm^2 with ease, have been studied widely. A flat cathode structure making use of an avalanche breakdown in a semiconductor and a tunnel effect in a dielectric isolation film or Schottky barrier has also been studied.

[0004] An example of an electron pulse emission device having the flat cathode structure of prior art will be described below. FIG. 6 is a cross-sectional view of a main portion of an electron pulse emission device of prior art.

[0005] As shown in FIG. 6, the electron pulse emission device of prior art comprises a first electrode 2 and a second electrode 4 between which a ferroelectric layer 3 is sandwiched and the second electrode 4 has openings 4a to expose the surface of the ferroelectric layer 3. In this structure, by rapidly alternating polarization in the ferroelectric layer 3 with application of a pulse voltage from an AC pulse power supply 7, a method of pulsed emission of electrons bound by polarization charges on the surface of the ferroelectric layer 3 has been attempted, which achieved a current density of 1 A/cm^2 and above (e.g., H. Gundl et al., Appl. Phys. Lett., Vol. 54, p. 2071, 1989).

[0006]

[Problems to be Solved by the Invention] However, the above

needle electrode structure of prior art has had the following problems: currents converging at the tips of the cathodes cause the tips to evaporate and emission current characteristics change over time; and the tips adsorb and release gas, which destabilizes the emission current characteristics.

[0007] On the other hand, the flat cathode structure making use of the avalanche breakdown and the tunnel effect has had a problem of high operating voltage because a high electric field is required for electron emission. Furthermore, most of micro vacuum tubes employing these cold cathodes operate on DC and, hence, have had a problem that a space-charge limitation effect saturates the emission electron current.

[0008] If only instantaneous current values are brought into question, this space-charge limitation effect can be avoided by pulsed emission of electrons into space. One example of the method of avoiding this space-charge limitation is electron emission from the surface of a ferroelectric layer, taking advantage of polarization inversion in the ferroelectric layer (e.g., H. Gundl et al., Appl. Phys. Lett., Vol. 54, p. 2071, 1989 and JP-A No. 325777/1993). However, the quantity of electrons emitted by this method is only at most the quantity of charged electrons coupled with polarization charges in the ferroelectric layer and, therefore, a high-density emission electron current cannot be expected. Because electrons are emitted from the surface of the ferroelectric layer, a problem that electron emission characteristics are destabilized by gas adsorption and release has also been presented.

[0009] To solve this problem, the inventors devised an electrode structure to stabilize the electron emission characteristics, wherein the surface of the ferroelectric layer is covered with a metal electrode and electrons are drawn by electric field application between the electrode and a trigger plate separated from this metal electrode via an isolation film (refer to JP-A No. 259304/1994). However, this structure improved the electron emission characteristics, but posed other problems that the isolation film between the metal electrode and the trigger plate must be non-conductive with a high dielectric strength and complicated circuitry must be made to drive this device.

[0010] The present invention is intended to solve the above problems associated with the prior art and its object is to provide an electron pulse emission device and a display device which are free from the space-charge limitation effect, are capable of achieving a high-density electron emission current by pulsed emission of electrons on a low operating voltage, and have a flat cathode structure with less characteristic variation and deterioration.

[0011]

[Means for Solving the Problems] To achieve the above object, according to one aspect (claim 1) of the present invention, there is provided an electron pulse emission device which comprises a supporting substrate, a first electrode formed on the supporting substrate, a ferroelectric layer formed on top of the first electrode, a second electrode formed on top of the

ferroelectric layer without being in contact with the first electrode, a third electrode facing toward the second electrode across a space, a means for applying a positive DC bias with regard to the first electrode to the third electrode, and a means for applying an AC pulse voltage between the first electrode and the second electrode to induce polarization inversion in the ferroelectric layer. The electron pulse emission device is characterized by intermittently emitting electrons from the surface of the second electrode toward the third electrode.

[0012] According to another aspect (claim 3) of the present invention, there is provided a display device which comprises a supporting substrate, a plurality of first electrodes formed on the supporting substrate, a ferroelectric layer formed on top of the first electrodes, a plurality of second electrodes formed on top of the ferroelectric layer without being in contact with the first electrodes and in an orthogonal direction to the first electrodes, and an isolation layer formed on top of the second electrodes, the isolation layer having openings at the intersections of the plurality of first electrodes and the plurality of second electrodes. The supporting substrate is placed opposite to a transparent substrate across a space, the transparent substrate facing toward the second electrodes across the space and having a transparent conductive layer and a phosphor layer formed thereunder. The display device further comprises a means for applying a positive DC bias with regard to the first electrodes to the transparent conductive layer and a means for applying an AC pulse voltage between each first

electrode and each second electrode to induce polarization inversion in the ferroelectric layer. The display device is characterized by intermittently emitting electrons from the exposed surfaces of the second electrodes toward the transparent conductive layer.

[0013]

[Function] The electron pulse emission device configured as described above can make use of not only electrons stored as capacitance coupled to the second electrode, but also electrons bound to the level of the interface between the second electrode and the ferroelectric layer, and electrons bound to fault levels in the ferroelectric layer as emission electrons, and, therefore, is capable of producing a high-density emission current.

[0014] A p-type diffusion layer may be formed as the first electrode on an n-type silicon substrate as the supporting substrate. In this structure, electrons injected from the pn junction can also be used as emission electrons and a higher-density emission current can be produced.

[0015] If the ferroelectric layer that is, for example, about 200 nm thick is formed, a voltage as low as ±5 V is enough to induce polarization inversion in the ferroelectric layer and electrons can be emitted with a low voltage. Because electrons are emitted from the surface of a flat structure of the second electron formation, an electron pulse emission device in which emission current convergence does not occur and which is less susceptible to gas adsorption and release can be realized. Its

operation can be effected simply by applying an AC pulse voltage between the first electrode and the second electrode and, therefore, circuitry required for the operation is simplified.

[0016] By employing the transparent substrate laminated with the transparent conductive layer which is formed as the third electrode in the above electron pulse emission device and further laminated with the phosphor layer, a thin display device capable of operating on a low voltage can be realized.

[0017]

[Preferred Embodiments] Preferred embodiments of the electron pulse emission device of the present invention will be described hereinafter with reference to the accompanying drawings.

[0018] FIG. 1 is a cross-sectional view of an electron pulse emission device according to a first embodiment of the present invention. In FIG. 1, reference numeral 1 denotes a supporting substrate such as a silicon substrate or glass substrate; 2 denotes a first electrode which consists of a platinum film; 3 denotes a ferroelectric layer which is made of zirconium titanate and is 200 nm thick and; 4 denotes a second electrode which consists of a platinum film and is 10 nm thick; and 5 denotes a third electrode which is made of aluminum, wherein the second electrode 4 and the third electrode 5 are separated by a gap of about 1 mm. Reference numeral 6 denotes a DC bias power supply and 7 denotes an AC pulse power supply and these power supply elements constitute a part of a drive circuit to actuate the electron pulse emission device.

[0019] Operation of the electron pulse emission device

configured as above will be explained below. First, a positive pulse voltage with regard to the first electrode 2 is applied between the first electrode 2 and the second electrode 4 to charge a capacitor consisting of the first electrode 2, ferroelectric layer 3, and second electrode 4. At this time, electrons are stored in the second electrode 4. Then, when a negative pulse voltage with regard to the first electrode 2 is applied between the first electrode 2 and the second electrode 4, polarization inversion takes place in the ferroelectric layer 3. By the DC bias 6 application, the electrons are emitted from the second electrode 4 toward the first electrode 5.

[0020] The above operation will be further explained, using electron energy band diagrams. FIG. 2A is an electron energy band diagram when the positive pulse voltage with regard to the first electrode is applied to the second electrode. FIG. 2B is an electron energy band diagram when the negative pulse voltage with regard to the first electrode is applied to the second electrode. In these figures, reference numeral 21 denotes the electron energy band of the first electrode 2; 22 denotes the electron energy band of the ferroelectric layer 3; 23 denotes the electron energy band of the second electrode 4; 24 denotes a vacuum level; 25 denotes a Fermi level; 26 denotes an electron, capacitance coupled to the second electrode 4; 27 denotes an electron bound to the level of the interface between the second electrode 4 and the ferroelectric layer 3; and 28 denotes an electron bound to a fault level in the ferroelectric layer 3. The following explanation will focus on electrons only

as units of charge.

[0021] As shown in FIG. 2A, when the positive pulse voltage with regard to the first electrode 2 is applied between the first electrode 2 and the second electrode 4, electrons 26, capacitance coupled to the second electrode 4, are stored in the second electrode 4, electrons 27 bound to the interface level are stored on the interface between the second electrode 4 and the ferroelectric layer 3, and electrons 28 bound to fault levels are stored in the ferroelectric layer 3. Then, as shown in FIG. 2B, when the negative pulse voltage with regard to the first electrode 2 is applied between the first electrode 2 and the second electrode 4, polarization inversion occurs in the ferroelectric layer 3. By an electric field generated by a polarization charge resulting from the polarization inversion, the electrons 27 bound to the interface level jump out toward the vacuum level 24. Furthermore, accelerated by the electric field applied to the ferroelectric layer 3, the electrons 28 bound to fault levels in the ferroelectric layer 3 hop from one to another fault level and jump out toward the vacuum level 24.

[0022] Next, an electron pulse emission device according to a second embodiment of the present invention will be described with reference to the accompanying drawings.

[0023] FIG. 3 is a cross-sectional view of the electron pulse emission device of the second embodiment. In FIG. 3, reference numeral 31 denotes an n-type silicon substrate; 32 denotes a first electrode which consists of a p-type diffusion layer; 33 denotes a ferroelectric layer which is made of zirconium

titanate and is 200 nm thick; 34 denotes a second electrode which consists of a platinum film and is 10 nm thick; 35 denotes a third electrode which is made of aluminum, wherein the second electrode 34 and the third electrode 35 are separated by a gap of about 1 mm; 36 denotes a DC bias power supply; and 37 denotes an AC pulse power supply. The first electrode 32 forms a pn junction with the n-type silicon substrate 31. The AC pulse power supply 37 is electrically connected to the first electrode 32 and the polarity of voltage that is applied between the first electrode 32 and the second electrode 34 is opposite to the polarity of voltage that is applied between the first electrode 32 and the n-type silicon substrate 31.

[0024] Operation of the electron pulse emission device of the second embodiment configured as above will be explained below.

[0025] FIG. 4A is an electron energy band diagram when the DC bias power supply and the AC pulse power supply are disconnected. FIG. 4B is an electron energy band diagram when the DC bias power supply and AC pulse power supply 37 are connected and a positive pulse voltage is applied to the first electrode 32. FIG. 4C is an electron energy band diagram when a negative pulse voltage is applied to the first electrode 32. In these figures, reference numeral 41 denotes the electron energy band of the pn junction; 42 denotes the electron energy band of the ferroelectric layer; 43 denotes the electron energy band of the second electrode 34; 44 denotes a vacuum level; 45 denotes a Fermi level; 46 denotes an electron, capacitance coupled to the second electrode 34; 47 denotes an electron bound to the level

of the interface between the second electrode 34 and the ferroelectric layer 33; 48 denotes an electron bound to a fault level within the ferroelectric layer 33; and 49 denotes an electron injected into the first electrode 32 from the n-type silicon substrate 31.

[0026] When a bias voltage is applied and a positive pulse voltage is applied to the first electrode 32, as shown in FIG. 2A, electrons 46, capacitance coupled to the second electrode 43 are stored in the second electrode 43, electrons 47 bound to the interface level are stored on the interface between the second electrode 34 and the ferroelectric layer 33, and electrons 48 bound to fault levels are stored in the ferroelectric layer 33. Moreover, because the pn junction is forward biased, electrons 49 are diffusely injected into the first electrode 32 from the n-type silicon substrate 31 and part of these electrons become electrons 47 bound to the level of the interface between the ferroelectric layer 33 and the first electrode 32.

[0027] Then, when a negative pulse voltage is applied to the first electrode 32, as shown in FIG. 4C, polarization inversion occurs in the ferroelectric layer 33. By an electric field generated by a polarization charge resulting from the polarization inversion, the electrons 47 bound to the interface level jump out toward the vacuum level 44. Furthermore, accelerated by the electric field applied to the ferroelectric layer 33, the electrons 48 bound to fault levels in the ferroelectric layer 33 hop from one to another fault level and

jump out toward the vacuum level 44. In addition, the electrons 47 bound to the interface level between the first electrode 32 and the ferroelectric layer 33 are also accelerated by the electric field and emitted toward the vacuum level 44.

[0028] While the electron pulse emission device of the second embodiment employing the n-type silicon substrate and the p-type diffusion layer as the first electrode and making use of the pn junction has been discussed, a similar electron pulse emission device can be constructed by forming an n-type well in a p-type silicon substrate and forming a p-type diffusion layer that serves as the first electrode in the n-type well. If the pn junction is not used, in a possible embodiment of the invention, an n-type diffusion layer may be formed in a p-type silicon substrate and used as the first electrode.

[0029] Next, a display device according to one embodiment of the present invention will be described with reference to the accompanying drawing. FIG. 5 is a three-dimensional cross-sectional view of the display device. In FIG. 5, reference numeral 51 denotes an n-type silicon substrate; 52 denotes a first electrode which consists of a p-type diffusion layer; 53 denotes a ferroelectric layer such as PZT; 54 denotes a second electrode consisting of a platinum film or the like, formed so as to intersect the first electrodes 52 orthogonally; 55 denotes an isolation layer which consists of a silicon oxide film or the like; 56 denotes an opening made in the isolation layer 55; 57 denotes a phosphor layer; 58 denotes a third electrode which consists of a transparent conductive layer; 59 denotes a

transparent substrate; 60 denotes a DC bias power supply; and 61 denotes an AC pulse power supply. The first electrodes 52 and the second electrodes 54 are assumed connected via switches omitted from the drawing to the AC-pulse power supply 61. As shown in FIG. 5, the display device of this embodiment is configured such that many openings for emitting electrons are provided at the top of the n-type silicon substrate 51 and the transparent substrate 59 with the phosphor layer 57 and the transparent conductive layer 58 formed under it is placed opposite to the top of the n-type silicon substrate 51, both substrates and their peripheries being vacuum sealed.

[0030] Specifically, numbers of first electrodes 51 disposed in parallel on the n-type silicon substrate 51 and numbers of second electrodes 54 disposed in parallel on the ferroelectric layer 53 are placed at right angles to each other. The numbers of second electrodes 54 are electrically isolated from each other by the isolation layer 55 consisting of the silicon oxide film with openings 56 for emitting electrons into a vacuum. The first electrodes 52 and the second electrodes 54 are terminated via the switches (not shown) at the AC pulse power supply 61. On the other hand, the third electrode 58 which catches emitted electrons biased by the DC bias voltage supply 60 with regard to the AC pulse power supply 61 is the transparent conductive layer formed on the inside of the transparent substrate 59 which is placed opposite to the electron emission surface across a space from the openings 56. As the material of the third electrode, for example, indium oxide (ITO) or the like is used.

Furthermore, in this embodiment, the transparent conductive layer 58 surface on which electrons arrive is coated with phosphor 57. A consistent gap between the silicon substrate 51 and the transparent substrate 59 can be maintained by inserting spacers between the transparent substrate 59 and isolation layer 55.

[0031] Operation of the display device configured as above will be explained below. First, a capacitor consisting of each first electrode 52, the ferroelectric layer 53, and each second electrode 54 is charged and discharged by the AC pulse power supply 61 in the same way as described for the electron pulse emission device shown in FIG. 3. Electron emission occurs in each of the points of grids formed by the first electrodes 52 and the second electrodes 54 disposed at right angles to each other. By a combination of the On and Off states of the switches (not shown) respectively connected to the first electrodes 52 and the second electrodes 54, the grid points are selected and deselected. Electrons emitted from the opening 56 at any grid point thus selected are accelerated by the DC bias power supply 60 and arrive on the third electrode 58. In this embodiment, because the third electrode 58 surface is coated with the phosphor 57, the accelerated electrons hit against the phosphor 57, thereby causing the phosphor to emit light. In other words, any point on the inside of the transparent substrate 59 can be selected to emit light and, therefore, this display device can be used as a flat image display device.

[0032] While the display device of the above embodiment

employing the p-type diffusion layer formed on the n-type silicon substrate 51 as the first electrodes 52 has been discussed, which is an example of efficiency enhancement through the use of the pn junction, the diffusion layer may be either p-channel type of n-channel type if it is simply used for wiring. A similar display device can be constructed by using an insulative substrate instead of the semiconductor substrate, forming a plurality of first electrodes made of a conductive material on the insulative substrate, forming the ferroelectric layer to cover the first electrodes, and forming second electrodes on the ferroelectric layer so as to intersect the first electrodes orthogonally.

[0033] While the display device of the above embodiment employing the second electrodes consisting of the platinum film has been discussed, a metal with a low work function other than platinum may be used or the surface of a low resistive metal may be coated with a substance that is of a high electron emission efficiency such as magnesium oxide (MgO) and cesium (Cs); thereby, a display device comprising an electron pulse emission device with a higher electron emission efficiency can be constructed.

[0034] To make the display device capable of displaying in color, phosphor film partitions for emitting different colors corresponding to the intersections of the first electrodes 52 and the second electrodes 54 may be formed on the transparent substrate 59 or a phosphor film 57 to emit white light may be selected and a mosaic color filter superposed on the transparent

substrate 59. At this time, the first electrodes 52 and the second electrodes 54 should intersect such that the intersections in a column (or row) are a half pitch off the positions of the intersections in an adjacent column (or row), thereby enabling a bright color display.

[0035] If a monocrystalline silicon substrate is used as the substrate, the electrodes can be formed by using a normal method of fabricating semiconductor devices and a high performance drive circuit can be formed in the periphery of a display unit. Thus, a small and high performance display device can be constructed.

[0036] If a transparent substrate on which a polycrystalline silicon film or amorphous silicon film is formed is used as the substrate, a large screen display device can be constructed, though its performance is somewhat lower than the display device employing the monocrystalline silicon substrate.

[0037]

[Effect of the Invention] The present invention provides an electron pulse emission device comprising a first electrode formed on a supporting substrate, a ferroelectric layer formed on top of the first electrode, a second electrode formed on top of the ferroelectric layer without being in contact with the first electrode, and a third electrode placed opposite to the second electrode across a space. By emitting electrons stored as capacitance coupled to the electrode, electrons bound to the level of the interface between the electrode and the ferroelectric layer, and electrons bound to fault levels in the

ferroelectric layer, an electron pulse emission device that produces a high-density emission current with a low voltage can be realized. If the ferroelectric layer is, for example, about 200 nm thick, a voltage as low as ±5 V is enough to induce polarization inversion in the ferroelectric layer and the device can operate on a low voltage.

[0038] In a preferred embodiment, an n-type silicon substrate is used and a p-type diffusion layer is formed as the first electrode, on top of which the ferroelectric layer and second electrode are formed in order, and the third electrode is positioned above them. In this structure, electrons injected from the pn junction can also be used as emission electrons and a higher-density emission current can be produced.

[0039] Electrons are emitted from the surface of a flat metal or oxide structure and an electron pulse emission device in which emission current convergence does not occur and which is less susceptible to gas adsorption and release can be realized.

[0040] Through application of the above electron pulse emission device, a very thin display device can be realized in which the third electrode is coated with a phosphor layer and the phosphor layer emits light when excited by emitted electrons.

[0041] In another embodiment, a monocrystalline silicon substrate is used as the substrate of the display device and a drive circuit can be formed integrally with the display unit in its periphery. This can reduce the number of input terminals

of the display device and simplify external circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of an electron pulse emission device according to a first embodiment of the present invention;

FIG. 2A is an electron energy band diagram when a positive pulse voltage with regard to a first electrode is applied to a second electrode in the electron pulse emission device of the first embodiment;

FIG. 2B is an electron energy band diagram when a negative pulse voltage with regard to the first electrode is applied to the second electrode in the electron pulse emission device of the first embodiment;

FIG. 3 is a cross-sectional view of an electron pulse emission device according to a second embodiment of the present invention;

FIG. 4A is an electron energy band diagram when a DC bias voltage and an AC pulse voltage are not applied in the electron pulse emission device of the second embodiment;

FIG. 4B is an electron energy band diagram when a DC bias voltage is applied and a positive pulse voltage is applied to a p-type diffusion layer in the electron pulse emission device of the second embodiment;

FIG. 4C is an electron energy band diagram when a DC bias voltage is applied and a negative pulse voltage is applied to the p-type diffusion layer in the electron pulse emission device of the second embodiment;

FIG. 5 is a three-dimensional cross-sectional view of a display device according to one embodiment of the present invention; and

FIG. 6 is a cross-sectional view of a main portion of an electron pulse emission device of prior art.

[Description of Reference Numerals]

1 Supporting plate

2 First electrode

3 Ferroelectric layer

4 Second electrode

5 Third electrode

FIG. 1

1 SUPPORTING PLATE

2 FIRST ELECTRODE

3 FERROELECTRIC LAYER

4 SECOND ELECTRODE

5 THIRD ELECTRODE

FIG. 2

FIG. 6

FIG. 3

FIG. 4

FIG. 5

55 ISOLATION LAYER

56 OPENING FOR EMISSION

57 PHOSPHOR

59 GLASS PLATE